AMENDMENTS TO THE SPECIFICATION

IN THE ABSTRACT

Please replace the abstract in the above-identified application with the following:

—A decoder ~~and a decoding method can perform~~for performing log-sum corrections by means of a linear approximation, putting stress on speed, with a reduced circuit dimension without adversely affecting the decoding performance of the circuit. The decoder ~~comprises a linear approximation circuit 68 added to obtain log likelihoods and adapted to compute the correction term expressed by a one-dimensional function of a variable by linear approximation. The~~includes a linear approximation circuit ~~68~~ that computes the ~~correction term by~~ log-sum corrections ~~by means of linear approximation~~ using the function F = -a P - Q + b, where the coefficient -a ~~representing~~ represents the gradient of the function and the coefficient b ~~representing~~ represents the intercept and are expressed by a power exponent of 2. ~~More specifically, when the coefficients a and b are expressed respectively by -2 k and 2m -1, the linear approximation circuit 68 discards from the lowest bit the k-th lowest bits, bit-shifts the absolute value data P - Q and then inverts the m bits from the k+1 th lowest bit to the m+k-th lowest bit by means of inverter 91.~~—

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